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(54) **SEMICONDUCTOR DEVICE**

(57) Abstract:

PURPOSE: To make the redundancy test for a dynamic RAM and the like having a redundancy circuit efficient and to improve the reliability and the yield rate of products by realizing the redundancy circuit, which can artificially form the disconnected state of a fuse for each bit and can normality function when a power supply is turned ON.

CONSTITUTION: Fuses F1 and F2 are provided at unit-address memories URM0- URMi-2 in an X-system redundancy circuit XR on the like. One of the fuses F1 and F2 is coupled to the input terminal of a level-judging inverter N1 or N3, and the other is directly coupled to the power supply voltage of the circuit without going through a cut MOSFET. NOR gates NO1 and NO2 selectively fix the substantial output signal levels of these inverters to the same state when the corresponding fuse F1 or F2 is disconnected based on a test control signal RTM. The NOR gates NO1 and NO2 are provided at the rear stages of the level judging inverters N1 and N3.